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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,073	12/09/2003	Jia-Chong Ho	HOJ13001/EM	2765
23364	7590	10/11/2006	EXAMINER	
BACON & THOMAS, PLLC 625 SLATERS LANE FOURTH FLOOR ALEXANDRIA, VA 22314			TRAN, THANH Y	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/730,073

Applicant(s)

JIA-CHONG HO

Examiner

Thanh Y. Tran

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 August 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-10 and 16-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-10, and 16-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 6-7, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al (U.S. 2005/0127380) in view of Wahl et al (U.S. 4,321,163) and Shimizu et al (U.S. 5,892,706).

As to claim 1, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, comprising: a group II-VI compound ("ZnO") (see paragraph [0029]), the dopant is selected from group IIIA elements ("B, Al, Ga, In, Tl") (see paragraph [0029]).

Kawasaki et al does not disclose a group II-VI compound doped with a dopant ranging from 0.1 to 30 mol%. Wahl et al discloses in col. 4, lines 61-67 a compound doped with a dopant ranging from 0.1 to 30 mol% ("0.2 to 8 mole percent"). It should be noted that: "0.2 to 8 mole percent" falls in the range of 0.1 to 30 mol%. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the compound material of Kawasaki et al by using a rule of "from 0.1 to 30 mol%" for a dopant range of the compound as taught by Wahl et al for increasing the conductivity of the active layer of the thin film transistor device.

Art Unit: 2822

Kawasaki et al in view of Wahl et al does not disclose a precursor solution of the compound semiconductor material is prepared by a Sol-gel process.

Shimizu et al discloses in col. 7, lines 5-17 a precursor solution of the compound material is prepared by a Sol-gel process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kawasaki et al in view of Wahl et al by using a Sol-gel process as taught by Shimizu et al for a precursor solution of the compound semiconductor material for the purpose of easily obtaining/forming the film having large surface areas in the substrate (see col. 7, lines 5-17 in Shimizu et al).

As to claim 2, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the group II-VI compound is ZnO ("ZnO") (see paragraph [0029]).

As to claim 3, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the group IIIA elements ("B, Al, Ga, In, Tl") (see paragraph [0029]).

As to claim 6, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the thin film transistor device is composed of a gate electrode (14), a source electrode (12), a drain electrode (13), a dielectric layer (15), and a substrate (16) (see paragraph [0025]).

As to claim 7, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the gate electrode, the source electrode, or the drain electrode of the thin film transistor device is made of metals (channel layer is made of metal "conductive layer") (see paragraph [0063]).

As to claim 9, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the dielectric layer (15) of the thin film transistor device is made of a high dielectric constant (see paragraph [0030]).

As to claim 10, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the substrate is a glass/plastic substrate (see paragraph [0031]).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al (U.S. 2005/0127380) in view of Wahl et al (U.S. 4,321,163) and Shimizu et al (U.S. 5,892,706) as applied to claim 1 above, and further in view of Baek et al (U.S. 2003/0219920).

As to claim 5, Kawasaki et al in view of Wahl et al and Shimizu et al does not teach the active layer of the thin film transistor device is patterned by Micro Contact Printing.

Baek et al teaches in the paragraph [0043] the active layer of the thin film transistor device is patterned by Micro Contact Printing. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kawasaki et al in view of Wahl et al and Shimizu et al by using Micro Contact Printing process to form an active layer as taught by Baek et al for easily forming a pattern/layer on the substrate of the thin film transistor device.

Art Unit: 2822

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al (U.S. 2005/0127380) in view of Wahl et al (U.S. 4,321,163) and Shimizu et al (U.S. 5,892,706) as applied to claim 1 above, and further in view of Bai et al (U.S. 2004/0222412).

As to claim 8, Kawasaki et al in view of Wahl et al and Shimizu et al does not teach the dielectric constant of the dielectric layer is more than 3.

Bai et al teaches in the paragraph [0043] the dielectric constant of the dielectric layer is more than 3 ("at least about 3.5"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Kawasaki et al in view of Wahl et al and Shimizu et al by using a dielectric layer with a constant of more than 3 as taught by Bai et al for providing a high dielectric constant in order to lower the operating voltages of device while maintaining the same charge polarization (see paragraph [0005] in Bai et al).

5. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al (U.S. 2005/0127380) in view of Wahl et al (U.S. 4,321,163).

As to claim 16, Kawasaki et al discloses in figures 6A-6B a thin film transistor device comprising: a substrate (66); a gate electrode (69) deposited on the substrate (66); a dielectric layer ("gate insulating layer" 65) deposited on the gate electrode (69); a source electrode (62) and a drain electrode (63) deposited on the dielectric layer (65); and an active layer ("channel layer" 61) deposited on the gate electrode (69) and source electrode (62), wherein the active layer ("channel layer" 61) comprising: a group II-VI compound ("ZnO"/"Zinc oxide") (see

Art Unit: 2822

paragraphs [0029], [0030], and [0063]), the dopant is selected from group IIIA elements ("B, Al, Ga, In, Tl") (see paragraph [0029]).

Kawasaki et al does not disclose a group II-VI compound doped with a dopant ranging from 0.1 to 30 mol%.

Wahl et al discloses in col. 4, lines 61-67 a compound doped with a dopant ranging from 0.1 to 30 mol% ("0.2 to 8 mole percent"). It should be noted that: "0.2 to 8 mole percent" falls in the range of 0.1 to 30 mol%. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the compound material of Kawasaki et al by using a rule of "from 0.1 to 30 mol%" for a dopant range of the compound as taught by Wahl et al for increasing the conductivity of the active layer of the thin film transistor device.

As to claim 17, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the group II-VI compound is ZnO ("ZnO") (see paragraph [0029]).

As to claim 18, Kawasaki et al discloses in figures 1A-3 a compound semiconductor material for forming an active layer of a thin film transistor device, wherein the group IIIA elements ("B, Al, Ga, In, Tl") (see paragraph [0029]).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al (U.S. 2005/0127380) in view of Wahl et al (U.S. 4,321,163) as applied to claim 16 above, and further in view of Shimizu et al (U.S. 5,892,706).

Art Unit: 2822

As to claim 19, Kawasaki et al in view of Wahl et al does not disclose a precursor solution of the active layer is prepared by a Sol-gel process.

Shimizu et al discloses in col. 7, lines 5-17 a precursor solution of the compound material is prepared by a Sol-gel process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kawasaki et al in view of Wahl et al by using a Sol-gel process as taught by Shimizu et al for a precursor solution of the active layer for the purpose of easily obtaining/forming the film having large surface areas in the substrate (see col. 7, lines 5-17 in Shimizu et al).

#### ***Response to Arguments***

7. Applicant's arguments with respect to claims 1-3, 5-10, and 16-19 have been considered but are moot in view of the new ground(s) of rejection.

#### **Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

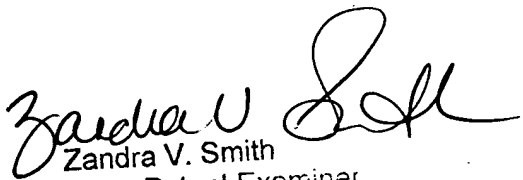
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

  
Zandra V. Smith  
Supervisory Patent Examiner  
2 Oct. 2006